S/N 09/256,643 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Leonard Forbes et al. Examiner: Unknown
Serial No.: 09/256,643 Group Art Unit: 2822
Filed: February 23, 1999 Docket: 303.324US2
Title: TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants further request that a copy of the 1449 form, initialed by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Under 37 C.F.R. §1.97(b)(3), it is believed that no fee or certificate is required with this Supplemental Information Disclosure Statement. **However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge any additional fees or credit any overpayment to Account No. 19-0743.**

The Examiner is invited to contact the Applicants' Representatives at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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Minneapolis, MN 55402
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Date 4/30/99 By _____
REM:lbc Robert E. Mates
Reg. No. 35,271

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on **April 30, 1999**.

Robert E. Mates _____
Name Signature

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Docket No.: 303.324US2
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Due Date: N/A
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Assistant Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.
X A Supplemental Information Disclosure Statement (1 pg.), Form 1449 (1 pg.), and copies of 3 cited references.
X Communication Concerning Co-Pending Applications (2 pgs.).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this Transmittal Letter and the paper, as described above, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on this 30th day of April, 1999.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

By: _____
Atty: Robert E. Mates
Reg. No. 35,271

Customer Number 21186

(GENERAL)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Leonard Forbes et al.	Examiner: Unknown	
Serial No.:	09/256,643	Group Art Unit: 2822	
Filed:	February 23, 1999	Docket: 303.324US2	
Title:	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE		

COMMUNICATION CONCERNING COPENDING APPLICATION

Assistant Commissioner for Patents
Washington, D.C. 20231

Applicants would like to bring to the Examiner's attention the following list of co-pending applications for the above-identified patent application.

Serial No.	Filing Date	Attorney Docket No.	Title
08/903,452	07/29/97	303.324US1	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE
09/138,294	08/21/98	303.353US2	TRANSISTOR WITH SILICON OXYCARBIDE GATE AND METHODS OF FABRICATION AND USE
08/902,843	07/29/97	303.354US1	DEAPROM HAVING AMORPHOUS SILICON CARBIDE GATE INSULATOR
09/135,413	08/14/98	303.354US2	DEAPROM HAVING AMORPHOUS SILICON CARBIDE GATE INSULATOR
09/134,713	08/14/98	303.354US3	DEAPROM HAVING AMORPHOUS SILICON CARBIDE GATE INSULATOR
08/902,098	07/29/97	303.355US1	DEAPROM AND TRANSISTOR WITH GALLIUM NITRIDE OR GALLIUM ALUMINUM NITRIDE GATE
09/140,978	08/27/98	303.355US2	DEAPROM AND TRANSISTOR WITH GALLIUM NITRIDE OR GALLIUM ALUMINUM NITRIDE GATE
09/141,392	08/27/98	303.355US3	DEAPROM AND TRANSISTOR WITH GALLIUM NITRIDE OR GALLIUM ALUMINUM NITRIDE GATE

Serial No.	Filing Date	Attorney Docket No.	Title
08/902,133	07/29/97	303.356US1	DYNAMIC ELECTRICALLY ALTERABLE PROGRAMMABLE READ ONLY MEMORY DEVICE
08/903,453	07/29/97	303.378US1	CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS
09/258,467	02/26/99	303.378US2	CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

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Robert E. Mates _____
Name Signature